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Park**

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(54) **METHOD FOR FABRICATING
SEMICONDUCTOR APPARATUS**

H01L 21/04 (2006.01)

H01L 27/10 (2006.01)

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(52) **U.S. Cl.**

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21/0455 (2013.01); **H01L 21/32139** (2013.01);
H01L 27/101 (2013.01); **H01L 29/0847**
(2013.01); **H01L 29/42356** (2013.01); **H01L**
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H01L 45/1233 (2013.01); **H01L 45/1675**
(2013.01)

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U.S.C. 154(b) by 0 days.

This patent is subject to a terminal dis-
claimer.

(58) **Field of Classification Search**

CPC H01L 27/11556; H01L 27/11551;
H01L 27/11578; H01L 29/7926; H01L
29/7889

See application file for complete search history.

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(56)

References Cited

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257/4

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* cited by examiner

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(30) **Foreign Application Priority Data**

May 30, 2014 (KR) 10-2014-0066071

(57)

ABSTRACT

A method for fabricating a semiconductor apparatus
includes forming a diffusion barrier film on a semiconductor
substrate, forming a first film on a semiconductor substrate
including a common source region, forming a second film on
the first film, forming a conductive film on the second film,
patterning the conductive film and the second film, to form
an active pattern, and patterning the first film and the
semiconductor substrate using the active pattern as a mask,
to form a pillar; and forming a gate electrode on an outer
circumference of the pillar.

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H01L 45/00 (2006.01)

H01L 29/423 (2006.01)

H01L 29/08 (2006.01)

H01L 21/02 (2006.01)

H01L 21/3213 (2006.01)

14 Claims, 6 Drawing Sheets

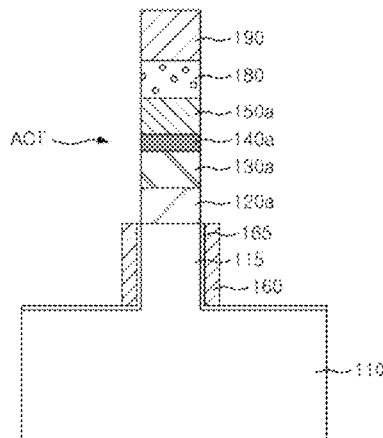


FIG. 1

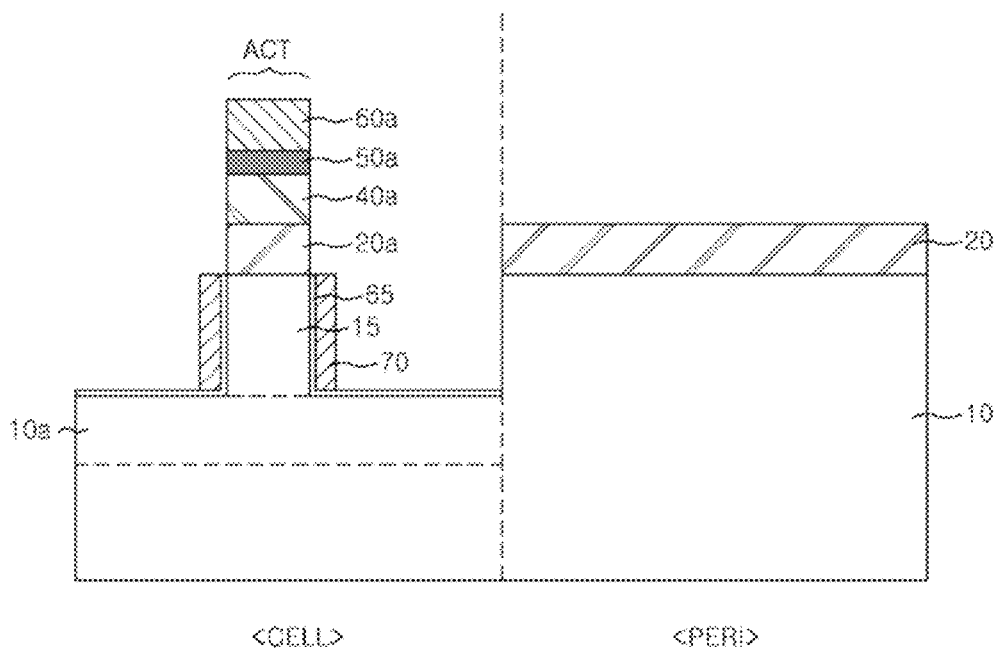


FIG. 2

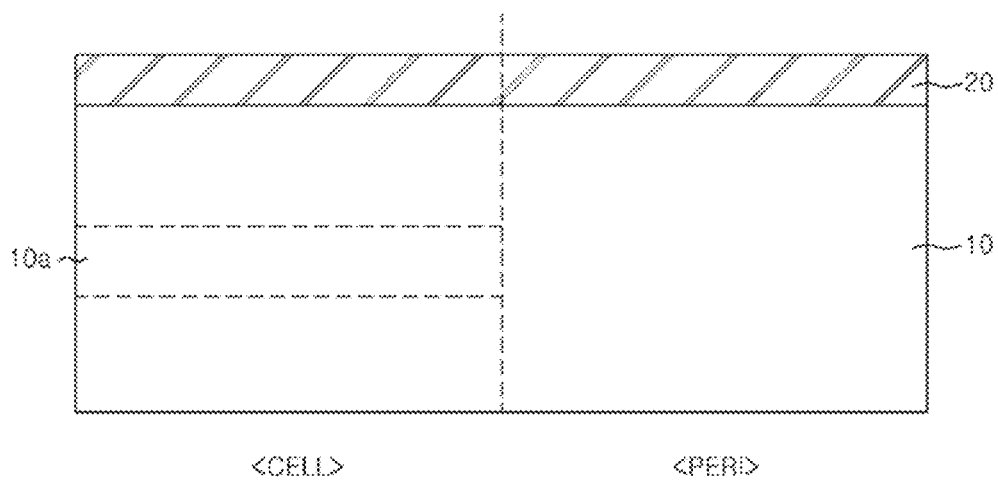


FIG.3

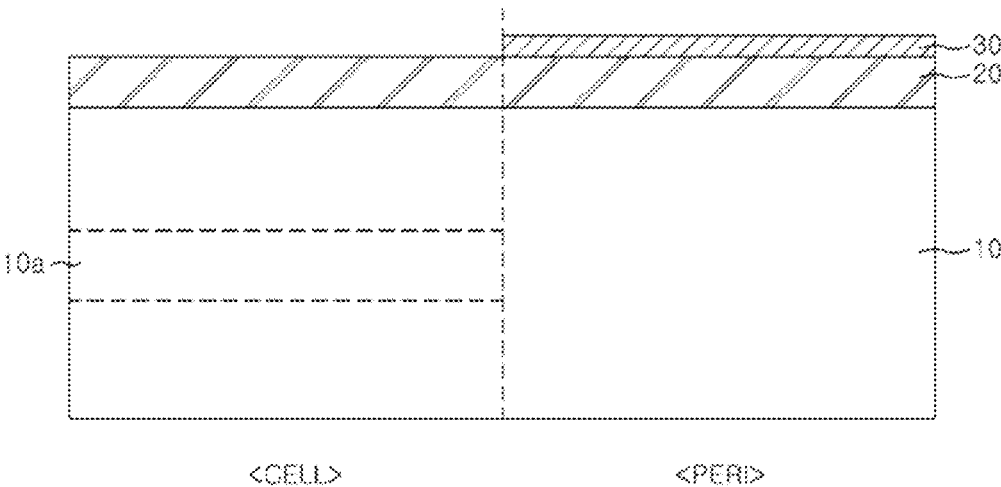


FIG.4

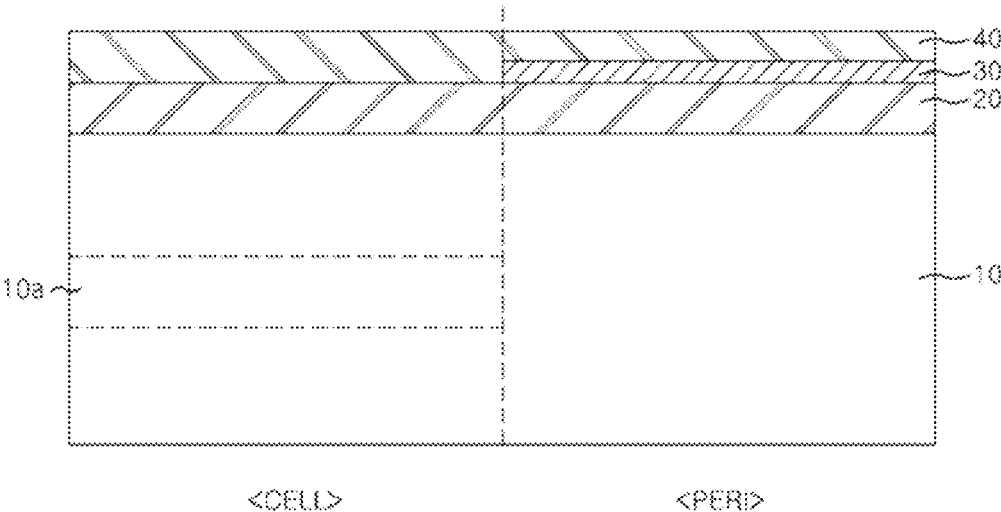


FIG.5

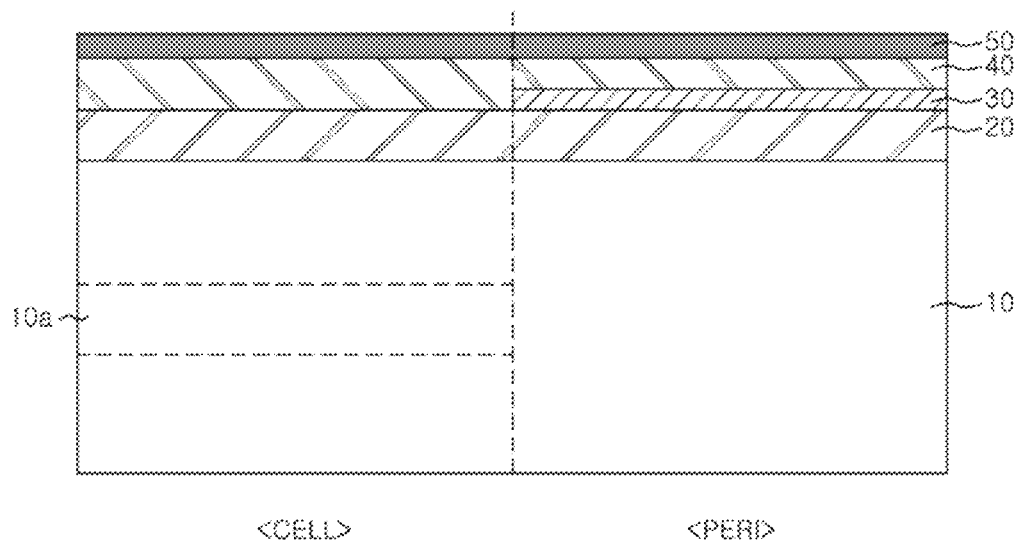


FIG.6

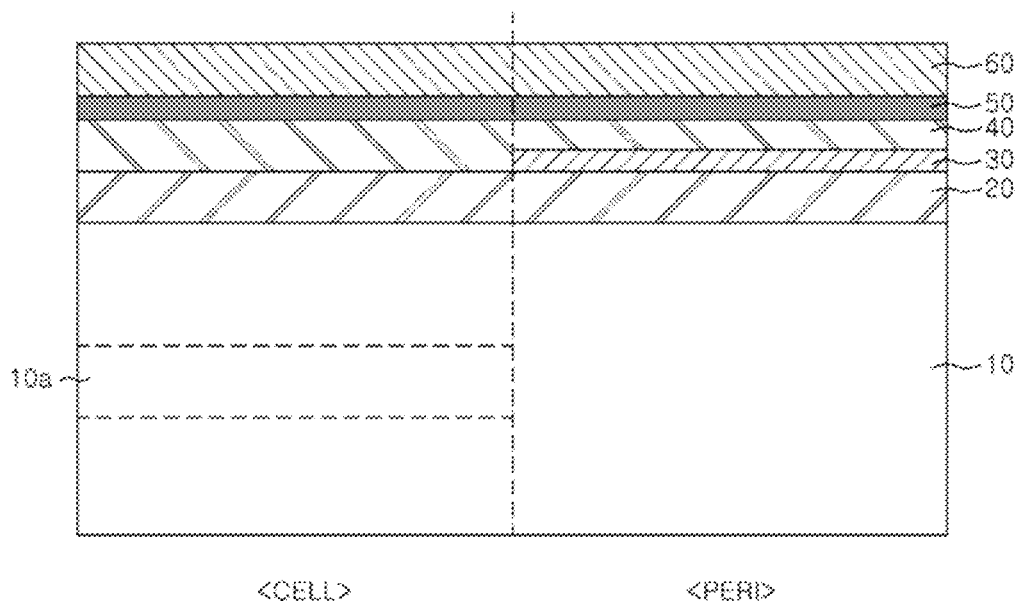


FIG. 7

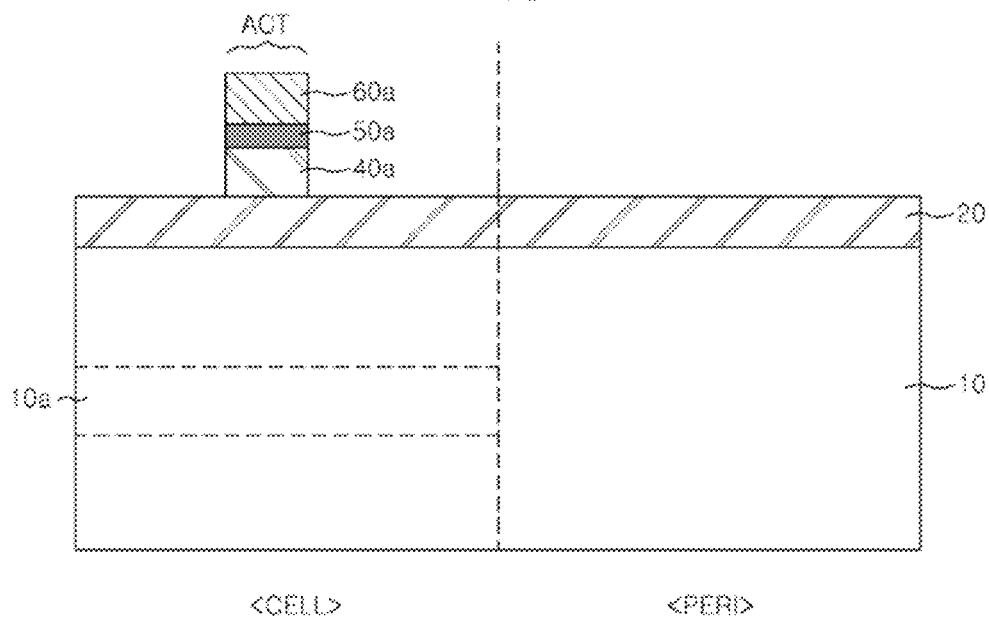
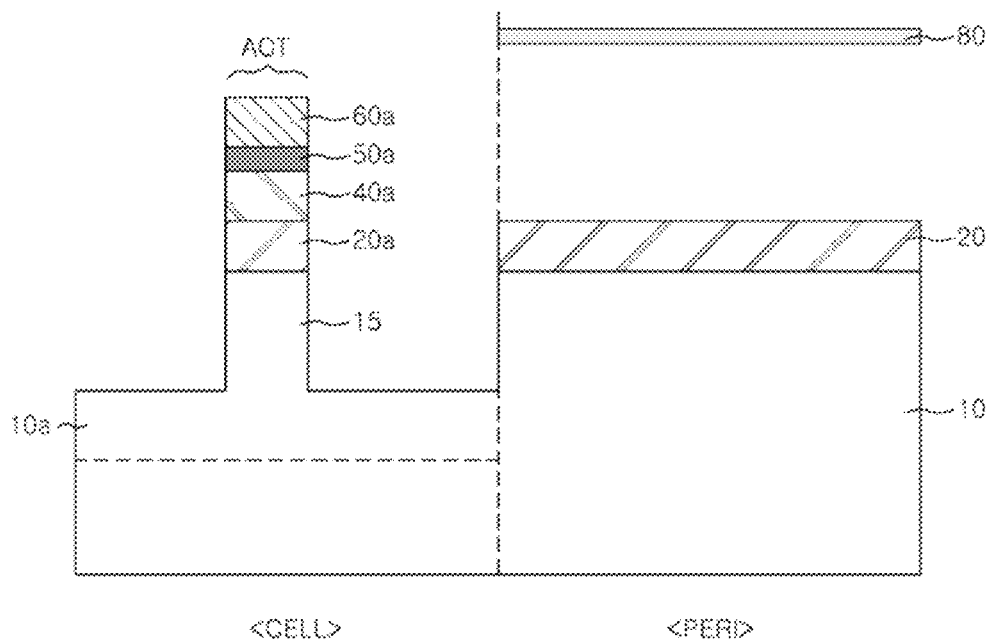


FIG. 8



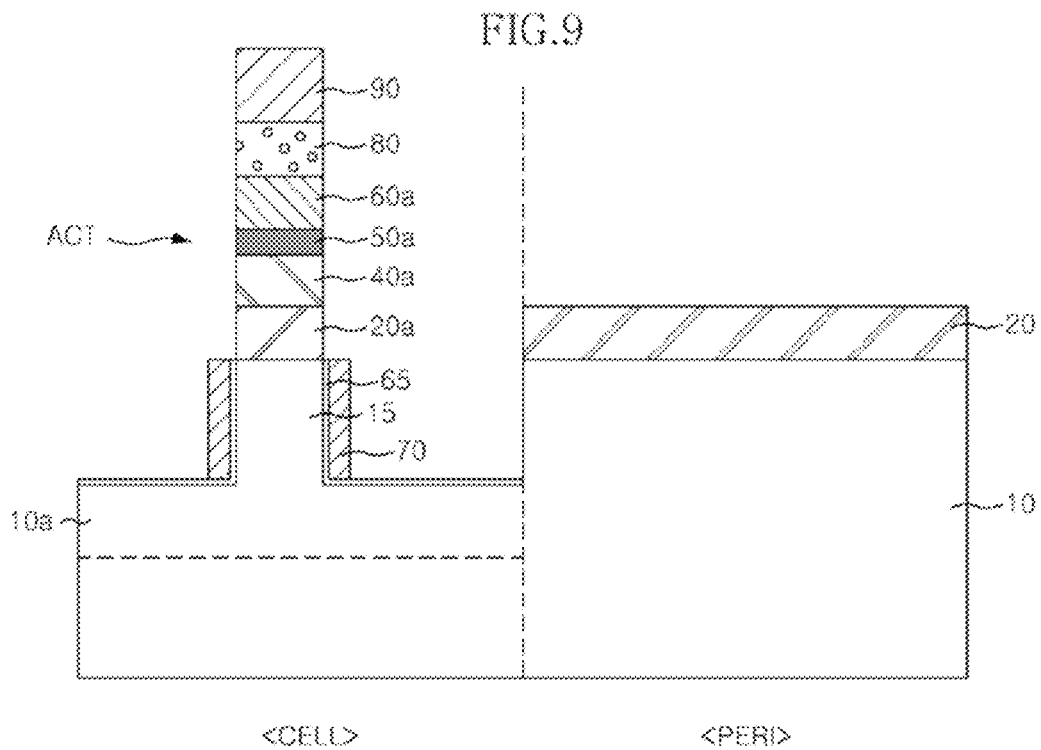


FIG.10

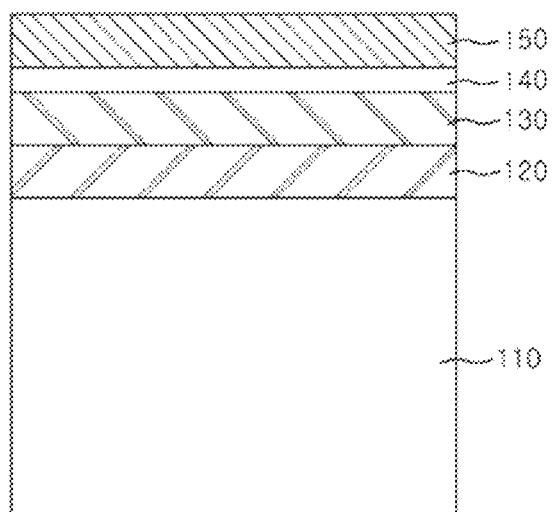


FIG. 11

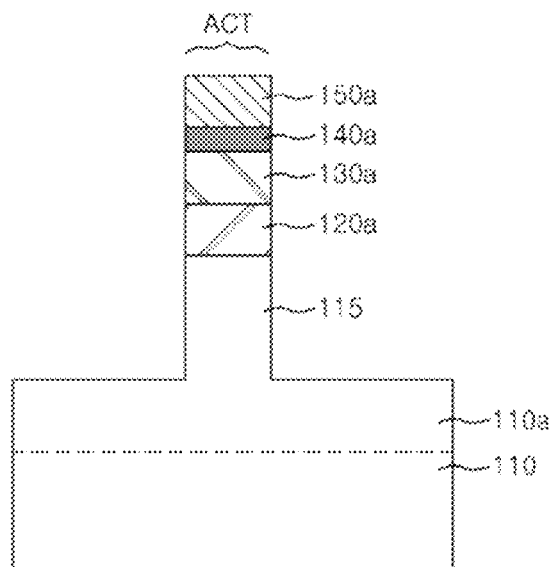
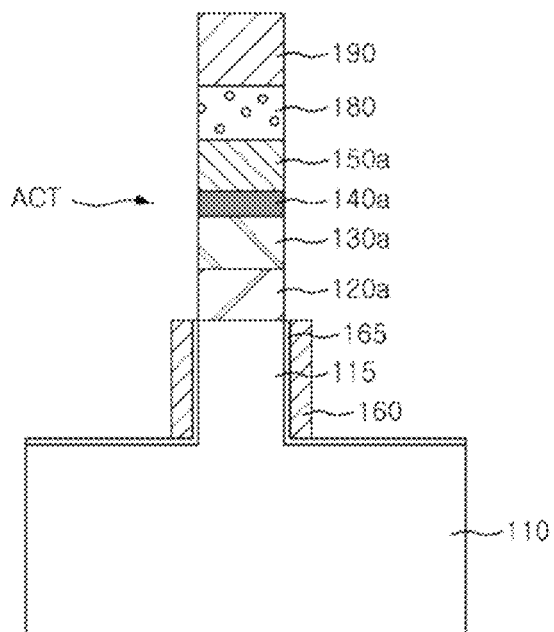


FIG. 12



1

METHOD FOR FABRICATING SEMICONDUCTOR APPARATUS

CROSS-REFERENCES TO RELATED APPLICATION

This application is a continuation-in-part of application Ser. No. 14/483,872, filed on Sep. 11, 2014, titled "METHOD FOR FABRICATING SEMICONDUCTOR APPARATUS", which claims priority under 35 U.S.C. 119 (a) to Korean application No. 10-2014-0066071, filed on May 30, 2014, in the Korean intellectual property Office. The disclosure of each of the foregoing applications is incorporated herein by reference in its entirety as set forth in full.

BACKGROUND

1. Technical Field

Various embodiments of the inventive concept relate to a method for fabricating a semiconductor apparatus having a vertical channel.

2. Related Art

Transistors, which are typical elements in semiconductor devices, include a gate, a source, and a drain. Transistors having two-dimensional (2D) structures may include a gate formed on a semiconductor substrate, and a source and a drain formed by doping the semiconductor substrate at both sides of the gate with impurities. The region between the source and the drain becomes the channel region of the transistor. The channel length of the transistor has a limit on how much its size can be reduced based on the linewidth of the gate. When the channel length is reduced below the limit, phenomena such as a short channel effect may occur that limit the ability of the transistor to properly function.

To overcome these limitations, vertical channel semiconductor devices have been used. In the vertical channel semiconductor devices, an active pattern is formed in a pillar form, and a source and a drain are located in lower and upper portions of the pillar to form the vertical channel, which is perpendicular to the surface of the semiconductor substrate.

In vertical channel semiconductor devices, a gate is extended in a line surrounding the pillar or in contact with either side of the pillar.

However, as the above-described vertical channel semiconductor devices are scaled down, there is increased fabrication difficulty. In particular, it is difficult to control the contact resistance between a vertical channel transistor and a lower electrode in a semiconductor device having a linewidth below 20 nm. Thus, there is a need for a method for fabricating semiconductor devices having stable contact resistance.

SUMMARY

An embodiment of the present invention is a method for fabricating a semiconductor apparatus. The method may include forming a first film on a semiconductor substrate including a common source region, forming a second film on the first film, forming a conductive film on the second film, patterning the conductive film and the second film, to form an active pattern, and patterning the first film and the semiconductor substrate using the active pattern as a mask, to form a pillar; and forming a gate electrode on an outer circumference of the pillar.

A second embodiment of the present invention is a method for fabricating a semiconductor apparatus. The

2

method may include providing a semiconductor substrate including a first region and a second region, forming a diffusion barrier film on the first and second regions of the semiconductor substrate, forming a semiconductor film with a conductive type on the first and second regions of the semiconductor substrate on which the diffusion barrier film is formed, forming an ohmic contact film on the semiconductor film, forming a conductive film on the ohmic contact film, forming a pillar structure by patterning the conductive film, the ohmic contact film, the semiconductor film, and the diffusion barrier film, and patterning the semiconductor substrate to a predetermined depth, resulting in a patterned semiconductor substrate, and forming a gate electrode surrounding an outer circumference of the pillar structure.

These and other features, aspects, and embodiments are described below in the section entitled "DETAILED DESCRIPTION".

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other aspects, features and advantages of the subject matter of the present disclosure will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view illustrating a semiconductor apparatus according to an embodiment of the inventive concept;

FIGS. 2 to 9 are cross-sectional views illustrating a method for fabricating a semiconductor apparatus according to an embodiment of the inventive concept; and

FIGS. 10 to 12 are cross-sectional views illustrating a method for fabricating a semiconductor apparatus according to another embodiment of the inventive concept

DETAILED DESCRIPTION

Exemplary embodiments will be described in greater detail with reference to the accompanying drawings. Variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments should not be construed as limited to the particular shapes illustrated herein but may include deviations in shapes that result, for example, from manufacturing. In the drawings, lengths and sizes of layers and regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements. When a layer is referred to as being "on" another layer or substrate, it can be directly on the other or substrate, or intervening layers may also be present. It is also noted that in this specification, "connected/coupled" refers to one component not only directly coupling another component but also indirectly coupling another component through an intermediate component. In addition, a singular form may include a plural form, and vice versa, as long as it is not specifically mentioned.

Embodiments of the inventive concept should not be construed as limiting, but rather illustrative. Although a few embodiments of the inventive concept will be shown and described, it will be appreciated by those of ordinary skill in the art that changes may be made to these exemplary embodiments without departing from the principles and spirit of the inventive concept.

Referring to FIG. 1, a semiconductor apparatus according to an embodiment of the inventive concept may include a semiconductor substrate 10 having a pillar 15, a gate electrode 70 surrounding a lateral surface of the pillar 15, and a

3

diffusion barrier layer 20a, a semiconductor layer 40a, an ohmic contact layer 50a, and a first electrode layer 60a sequentially stacked on a top surface of the pillar 15.

The diffusion barrier layer 20a may be formed of an undoped polysilicon material, and the semiconductor layer 40a may be formed of a doped polysilicon material. The semiconductor layer 40a may be formed of a material having the same conductivity type as a common source region 10a to be formed in the semiconductor substrate 10. For example, the diffusion barrier layer 20a may be a lightly doped drain region (Hereinafter, LDD region) and the semiconductor layer 40a may be a drain region of a vertical channel transistor.

The diffusion barrier layer 20a is formed between the semiconductor layer 40a and the pillar 15 to prevent impurities in the semiconductor layer 40a, which is formed of a doped polysilicon material, from being diffused to the pillar 15 used for a channel region. Further, the diffusion barrier layer 20a may mitigate a concentration of an electric field between the drain region 40a and the common source region 10a.

The pillar 15, the ohmic contact layer 50a, the first electrode layer 60a, and the gate electrode 70 have known structures, and thus a detailed description thereof will be omitted. The first electrode layer 60a may be a lower electrode of a variable resistive memory device.

The reference numeral 65 denotes a gate insulating layer located between the pillar 15 and the gate electrode 70.

Hereinafter, a method for fabricating a semiconductor apparatus according to an embodiment of the inventive concept will be described in detail with reference to FIGS. 2 to 9.

Referring to FIG. 2, a semiconductor substrate 10 including a cell region CELL and a peripheral region PERI is provided. The semiconductor substrate 10 may include a common source region 10a having a predetermined depth and formed on an upper surface thereof. The common source region 10a may be formed through implantation of a certain impurity, for example, an N⁺ type impurity. Further, the common source region 10a may be formed after a pillar structure (to be described later) is formed.

A diffusion barrier film 20 may be formed on the semiconductor substrate 10. The diffusion barrier film 20 may be formed of an undoped polysilicon material. For example, a material of the diffusion barrier film 20 is different from a material of the semiconductor substrate 10.

Referring to FIG. 3, a sacrificial film 30 may be formed on the peripheral region of the semiconductor substrate 10 in which the diffusion barrier film 20 is formed. The sacrificial film 30 is formed to control impurities which may diffuse to the peripheral region when a semiconductor film (see 40 of FIG. 4) is formed in a subsequent process. The sacrificial film 30 may include a titanium nitride (TiN) film, but the material for the sacrificial film 30 is not limited thereto.

Referring to FIG. 4, the semiconductor film 40 may be formed on the diffusion barrier film 20 and the sacrificial film 30. The semiconductor film 40 may be formed of a material having the same conductivity type as the common source region 10a. For example, when the common source region 10a is formed through the implantation of the N⁺ type impurity as described above, the semiconductor film 40 may also be doped with N⁺ type impurities. For example, a material of the semiconductor film 40 is different from a material of the diffusion barrier film 20. For example, the semiconductor film 40 may be formed of a doped polysilicon material and may be used as a drain region.

4

Referring to FIG. 5, a silicide film 50 is formed on the semiconductor film 40. The silicide film 50 may be formed through a series of processes of forming a transition metal material (not shown) on the semiconductor film 40, performing a heat treatment for reacting the transition metal material with the semiconductor film 40, and removing the transition metal material left after the heat treatment. The silicide film 50 may be used as an ohmic contact layer.

Referring to FIG. 6, a conductive film 60 may be formed on the silicide film 50. The conductive film 60 may include a TiN film, and the sacrificial film 30 but the material for the conductive film 60 is not limited thereto. The conductive film 60 may be used as a lower electrode in a variable resistive memory device.

Referring to FIG. 7, An active pattern ACT may be defined by forming a hard mask (not shown) formed on the conductive film 60. A step for forming the active pattern ACT may include patterning the conductive film 60, the silicide film 50, the semiconductor film 40, and the sacrificial film 30 using the hard mask. That is, the hard mask may be formed on the conductive film 60. The hard mask may be formed to define an active area of a vertical pillar transistor, in other words, a pillar. The conductive film 60, the silicide film 50 and the semiconductor film 40 are patterned by the hard mask. During the patterning step, the sacrificial film 40 is removed. Through the above-described process, a semiconductor layer 40a, an ohmic contact layer 50a, and a first electrode layer 60a of the embodiment may be formed. The hard mask is removed after the patterning step.

Referring to FIG. 8, a peri close mask 80 is formed on the peripheral region. Using the peri close mask 80 and the first electrode layer 60a, the diffusion barrier film 20 of the cell region other than the active pattern ACT is removed, and a portion of the semiconductor substrate 10 is recessed. For example, the semiconductor substrate 10 may be recessed to be exposed the common source region 10a. Through the process, a pillar 15 and a diffusion barrier layer 20a of the embodiment may be formed.

Referring to FIG. 9, a gate insulating film 65 may be formed on the exposed semiconductor substrate 10, that is, the gate insulating film 65 may be formed on a lateral surface of the pillar 15 and an exposed common source region 10a. A gate electrode 70 is formed to surround the pillar 15. The gate electrode 70 is insulated from the pillar 15 by the gate insulating film 65. Further, the gate electrode 70 is insulated from the common source region 10a by the gate insulating film 65.

The gate electrode 70 may be formed by gap-filling the cell region with a conductive material (not shown), spacer-etching the conductive material, and etching back the spacer-etched conductive material substantially to have the same height as a top surface of the pillar 15. The gate electrode 70 may include a TiN layer, but the material for the gate electrode 70 is not limited thereto.

A variable resistance layer 80 and a second electrode layer (or an upper electrode layer) 90 may be formed on the first electrode layer 60a to complete the semiconductor apparatus, for example, a variable resistive memory device. An insulating film (not shown) is gap-filled in the cell region other than the regions of the pillar structure including the pillar 15, the diffusion barrier layer 20a, the semiconductor layer 40a, the ohmic contact layer 50a, and the first electrode layer 60a, the variable resistance layer 80, the second electrode layer (or the upper electrode) 90, and the gate electrode 70. The process of gap-filling the insulating film is known technology, and thus a detailed description thereof will be omitted.

Hereinafter, a method for fabricating a semiconductor apparatus according to another embodiment of the inventive concept will be described in detail with reference to FIGS. 10 to 12.

Referring to FIG. 10, a diffusion barrier film 120, a semiconductor film 130, a silicide film 140, and a conductive film 150 are sequentially formed on a semiconductor substrate 110. A material of the diffusion barrier film 120 may be different from materials of the semiconductor substrate 110 and the semiconductor film 130.

For example, the diffusion barrier film 120 may be formed of an undoped polysilicon film but the material for the diffusion barrier film 120 is not limited thereto.

The semiconductor film 130 may include a semiconductor film having the same conductivity type as a common source region to be formed. For example, the semiconductor film 130 may be formed of a doped polysilicon film.

The silicide film 140 may be formed through a series of processes of forming a transition metal material (not shown) on the semiconductor film 130, performing a heat treatment for reacting the transition metal material with the semiconductor film 130, and removing the transition metal material left after the heat treatment.

The conductive film 150 may be used as a lower electrode in a variable resistive memory device. The process of forming the conductive film 150 is known technology, and thus a detailed description thereof will be omitted.

Referring to FIG. 11, an active pattern ACT is defined by patterning the conductive film 150, the silicide film 140, the semiconductor film 130, the diffusion barrier film 120, and a portion of the semiconductor substrate 110 to a predetermined depth. Through the process of defining the active pattern ACT, a pillar structure including a pillar 115, a diffusion barrier layer 120a, a semiconductor layer 130a, an ohmic contact layer 140a, and a first electrode layer 150a may be formed on the semiconductor substrate 110.

A common source region 110a may be formed by implanting impurities into the semiconductor substrate 110 after the pillar structure is completed. The process of forming the common source region 110a may be performed before the diffusion barrier film 120 is formed on the semiconductor substrate 110.

Referring to FIG. 12, a gate insulating film 165 may be formed on a lateral surface of the pillar 115 and an exposed semiconductor substrate 110, and a gate electrode 160 may be formed to surround an outer circumstance of the pillar 115.

The gate electrode 160 may be formed by gap-filling the semiconductor substrate, in which the pillar structure is formed, with a conductive material (not shown), spacer-etching the conductive material, and etching back the spacer-etched conductive material substantially to have the same height as a top surface of the pillar 115.

Although not shown in drawings, a variable resistance layer 180 and a second electrode layer (or an upper electrode layer) 190 may be formed on the first electrode layer 150a to complete the semiconductor apparatus, for example, a variable resistive memory device.

As described above, according to the embodiment of the inventive concept, a semiconductor layer is formed through a series of processes of forming a pillar structure by sequentially forming a diffusion barrier film, a semiconductor film, a transition metal film, and a conductive film on a semiconductor substrate, and patterning the conductive film, the transition metal film, the semiconductor film, and the diffusion barrier film, and the semiconductor substrate, and the semiconductor layer is used as a drain. Therefore, the

contact resistance of the drain may be easily controlled since the drain is not formed through ion implantation of impurities into an upper portion of the pillar.

According to the embodiment of the inventive concept, the pillar structure is formed by sequentially forming the diffusion barrier film, the semiconductor film, the transition metal film, and the conductive film on a semiconductor substrate, and patterning the conductive film, the transition metal film, the semiconductor film, and the diffusion barrier film, and thus the conductive film used as a lower electrode is formed on a flat plate. Therefore, the lower electrode may be formed to have a stable contact resistance without defects such as seams.

According to the embodiment of the inventive concept, the diffusion barrier layer and the semiconductor layer are formed of an undoped polysilicon material and a doped polysilicon material, respectively, on the pillar, and thus diffusion of impurities to the pillar may be prevented even when the height of the semiconductor layer is not large.

The above embodiment of the present invention is illustrative and not limitative. Various alternatives and equivalents are possible. The invention is not limited by the embodiments described herein. Nor is the invention limited to any specific type of semiconductor device. Other additions, subtractions, or modifications are obvious in view of the present disclosure and are intended to fall within the scope of the appended claims.

What is claimed is:

1. A method for fabricating a semiconductor apparatus, the method comprising:
 - forming a first film on a semiconductor substrate including a common source region;
 - forming a second film on the first film;
 - forming a conductive film on the second film;
 - patterning the conductive film and the second film, to form an active pattern; and
 - patterning the first film and the semiconductor substrate using the active pattern as a mask, to form a pillar; and
 - forming a gate electrode on an outer circumference of the pillar, wherein the first film includes an undoped polysilicon film and the second film includes a doped polysilicon film.
2. The method of claim 1, wherein a material of the first film is different from materials of the semiconductor substrate and the second film.
3. The method of claim 1, wherein the first film functions as a LDD (lightly doped drain) region and the second film functions as a drain.
4. The method of claim 1, wherein the forming of the gate electrode includes:
 - forming a gate insulating film on an exposed semiconductor substrate;
 - forming a conductive material on the semiconductor substrate in which the gate insulating film is formed;
 - spacer-etching the conductive material, resulting in a spacer-etched conductive material, to be formed on the outer circumference of the pillar; and
 - etching back the gate insulating film and the spacer-etched conductive material to have substantially the same height as a top surface of the patterned semiconductor substrate.
5. The method of claim 1, further comprising:
 - forming an ohmic contact film between the second film and the conductive film.
6. A method for fabricating a semiconductor apparatus, the method comprising:

7

providing a semiconductor substrate including a first region and a second region;
forming a diffusion barrier film on the first and second regions of the semiconductor substrate;

forming a semiconductor film with a conductive type on the first and second regions of the semiconductor substrate on which the diffusion barrier film is formed;
forming an ohmic contact film on the semiconductor film;
forming a conductive film on the ohmic contact film;
forming a pillar structure by patterning the conductive film, the ohmic contact film, the semiconductor film, and the diffusion barrier film, and patterning the semiconductor substrate to a predetermined depth, resulting in a patterned semiconductor substrate; and
forming a gate electrode surrounding an outer circumference of the pillar structure.

7. The method of claim 6, further comprising:

forming a common source region in the first region of the semiconductor substrate.

8. The method of claim 7, wherein the common source region has the same conductivity type as the semiconductor film.

9. The method of claim 6, wherein the diffusion barrier film includes an undoped polysilicon film.

10. The method of claim 9, wherein the semiconductor film includes a doped polysilicon film.

8

11. The method of claim 6, further comprising:

forming a sacrificial film on the diffusion barrier film of the second region between the forming the diffusion barrier film and the forming the semiconductor film.

12. The method of claim 11, wherein the forming the pillar structure:

patterning the conductive film, the ohmic contact film and the semiconductor film to have a structure of an active pattern, thereby forming a lower electrode, an ohmic contact pattern and a drain in the first region;

removing the sacrificial film of the second region;

patterning the diffusion barrier film using the lower electrode, as a mask, thereby forming a LDD region; and
recessing the semiconductor substrate using the lower electrode as the mask, thereby forming the pillar structure.

13. The method of claim 6, wherein the first region is a cell region and the second region is a peripheral region.

14. The method of claim 6, further comprising:

forming a variable resistance layer on a lower electrode of the pillar structure; and

forming an upper electrode on the variable resistance layer.

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